

I claim:

1. A semiconductor circuit in a semiconductor substrate, comprising:
a first input for feeding a first supply potential;
a second input for feeding a second supply potential higher than the first supply potential;
a device;
an output;
a parasitic pn-junction between the device and the semiconductor substrate, which is conductive at a first polarizing potential at the output smaller than the first supply potential or at a second polarizing potential at the output greater than the second supply potential; and
a protective circuit connected between the output and the pn-junction, and whose electric resistance at the first polarizing potential at the output and at the second polarizing potential at the output, respectively, is higher than at a normal operation potential at the output lying between the first supply potential and the second supply potential.
2. The semiconductor circuit of claim 1, wherein the semiconductor substrate is a p-doped semiconductor substrate and the protective circuit includes a pJFET, or wherein the semiconductor substrate is an n-doped semiconductor substrate and the protective circuit includes an nJFET.
3. The semiconductor circuit of claim 1, wherein the protective circuit includes a MOSFET the channel of which comprises the same conductivity type as the semiconductor substrate.
4. The semiconductor circuit of claim 1, wherein the semiconductor substrate is a p-doped semiconductor substrate and the pn-junction is conductive at the first polarizing potential at the output smaller than the first supply potential, or wherein the semiconductor substrate is an n-doped semiconductor substrate and the

parasitic pn-junction is conductive at the second polarizing potential at the output greater than the second supply potential.

5. The semiconductor circuit of claim 1, wherein the electric resistance of the protective circuit has a positive temperature coefficient.

6. The semiconductor circuit of claim 1, wherein the parasitic pn-junction is a pn-junction between the semiconductor substrate and a part of the device, which is non-conductive at a potential at the output greater than the first supply potential and smaller than the second supply potential.

7. The semiconductor circuit of claim 1, which is a linear or digital output stage connected to the output OUT.

8. A semiconductor circuit in a semiconductor substrate, comprising:
a first input for feeding a first supply potential;
a second input for feeding a second supply potential higher than the first supply potential;
an output stage coupled between the first and second input comprising an output and a parasitic pn-junction between the output stage and the semiconductor substrate, which is conductive at a first polarizing potential at the output smaller than the first supply potential or at a second polarizing potential at the output greater than the second supply potential; and
a protective circuit connected between the output and the pn-junction, and whose electric resistance at the first polarizing potential at the output and at the second polarizing potential at the output, respectively, is higher than at a normal operation potential at the output lying between the first supply potential and the second supply potential.
9. The semiconductor circuit of claim 8, wherein the semiconductor substrate is a p-doped semiconductor substrate and the protective circuit includes a pJFET, or wherein the semiconductor substrate is an n-doped semiconductor substrate and the protective circuit includes an nJFET.
10. The semiconductor circuit of claim 8, wherein the protective circuit includes a MOSFET having a channel of the same conductivity type as the semiconductor substrate.
11. The semiconductor circuit of claim 8, wherein the semiconductor substrate is a p-doped semiconductor substrate and the pn-junction is conductive at the first polarizing potential at the output smaller than the first supply potential, or wherein the semiconductor substrate is an n-doped semiconductor substrate and the parasitic pn-junction is conductive at the second polarizing potential at the output greater than the second supply potential.

12. The semiconductor circuit of claim 8, wherein the electric resistance of the protective circuit has a positive temperature coefficient.

13. The semiconductor circuit of claim 8, wherein the parasitic pn-junction is a pn-junction between the semiconductor substrate and a part of the device, which is non-conductive at a potential at the output greater than the first supply potential and smaller than the second supply potential.

14. The semiconductor circuit of claim 8, which is a linear or digital output stage connected to the output OUT.

15. The semiconductor circuit of claim 8, wherein the protective circuit is a field effect transistor whose drain source path is coupled between the output and the parasitic pn junction and whose gate is coupled through a diode with the output.

16. The semiconductor circuit of claim 15, further comprising a resistor between the output and the drain source path and a resistor between the gate and the diode.

17. The semiconductor circuit of claim 8, wherein the protective circuit is a first field effect transistor whose drain source path is coupled between the output and the parasitic pn junction and whose back gate is coupled through a diode with the output and whose front gate is coupled with a control circuit for pinching off the first field effect transistor in presence of the first polarizing voltage.

18. The semiconductor circuit of claim 17, wherein the control circuit comprises a second field effect transistor whose drain source path is coupled between the substrate and the front gate and wherein the second field effect transistor is controlled to be conductive if the voltage at the output is greater than the first supply voltage and a voltage source providing a predefined voltage to the front gate.

19. The semiconductor circuit of claim 17, wherein the semiconductor substrate is a p-doped semiconductor substrate and the first field effect transistor is a pJFET, or wherein the semiconductor substrate is an n-doped semiconductor substrate and the first field effect transistor is an nJFET.

20. The semiconductor circuit of claim 18 wherein second field effect transistor is a MOS transistor.